

**AMENDMENTS TO THE CLAIMS**

This listing of claims replaces all prior listing of claims in this application.

1. (Currently amended) A method of producing an imaging device, comprising:

forming a photosensitive region;

forming a diffusion region;

forming a gate structure between said photosensitive region and said diffusion region;

forming an insulating layer over the photosensitive region, the gate structure and the diffusion region; and

removing a first portion of the insulating layer over the diffusion region and a portion over said gate structure, leaving a forming at least one spacer at a adjacent to the diffusion region side of the gate structure, and leaving a second portion of the insulating layer over the photosensitive region and over a portion of said gate structure adjacent to said photosensitive region.

2. (Original) The method of claim 1, wherein the imaging device is a CMOS imager.

3. (Original) The method of claim 2, wherein the CMOS imager comprises a three-transistor, four-transistor, five-transistor, six-transistor, or seven-transistor architecture.

4. (Original) The method of claim 2, wherein the CMOS imager comprises at least one of a transfer gate, reset gate, row select gate, storage gate, dual conversion gate, and high dynamic range gate.

5. (Original) The method of claim 1, wherein the imaging device has periphery circuits.

6. (Original) The method of claim 1, wherein the imaging device is a CCD imager.

7. (Original) The method of claim 1, wherein the diffusion region is selected from the group consisting of a floating diffusion,  $N^+$  active area,  $P^+$  active area,  $N^-$  active area,  $P^-$  active area, and storage node diffusion.

8. (Original) The method of claim 7, wherein the first portion of the insulating layer is removed from over at least one of the floating diffusion,  $N^+$  active area,  $P^+$  active area,  $N^-$  active area,  $P^-$  active area, and storage node diffusion.

9. (Original) The method of claim 1, wherein the photosensitive region is selected from the group consisting of a photodiode, photogate, and photoconductor.

10. (Original) The method of claim 9, wherein the photodiode is a p-n-p photodiode.

11. (Original) The method of claim 1, wherein the insulating layer is selected from the group consisting of an oxide, nitride, oxide/nitride, and metal oxide.

12. (Currently amended) The method of claim 1, further comprising implanting dopant with the at least one spacer used as a mask.

13. (Canceled).

14. (Currently amended) The method of claim 1, wherein ~~the spacer is~~ spacers are left on both sides of at least one gate structure.

15. (Original) The method of claim 1, wherein the gate structure comprises a gate oxide and a gate conductor.

16. (Original) The method of claim 15, wherein the gate conductor comprises at least one of a polysilicon, silicide, metal, or combination of a polysilicon, silicide, and metal.

17. (Original) The method of claim 15, wherein the gate structure comprises a second insulator over the gate conductor.

18. (Original) The method of claim 17, wherein the second insulator comprises at least one of an oxide, nitride, metal oxide, or combination of an oxide, nitride, and metal oxide.

19. (Original) The method of claim 1, wherein the gate structure is an n-channel gate.

20. (Original) The method of claim 1, wherein the spacer is formed by a masked spacer etch.

21. (Currently amended) The method of claim ~~[[12]]~~ 20, wherein the mask used to define the masked spacer etch remains during the dopant implantation.

22. (Original) The method of claim 1, wherein the insulating layer has a thickness within the range of about 100 to about 1500 Angstroms.

23. (Original) The method of claim 22, wherein the insulating layer has a thickness within the range of about 200 to about 1000 Angstroms.

24. (Original) The method of claim 12, wherein the dopant is an n-type dopant.

25. (Currently amended) A method of producing an imaging device, comprising:

forming an array of photosensitive regions;

forming first and second sets of gate structures, the first set of gate structures being formed in said array and the second set of gate structures being formed in a periphery outside said array;

forming first and second sets of diffusion regions;

forming an insulating layer over the photosensitive ~~region~~ regions, the gate structures and the diffusion regions in the array and the periphery;

removing a first portion of the insulating layer over the first set of diffusion regions in the array, leaving a spacer on at least one side of at least one gate structure of the first set of gate structures in the array and leaving a second portion of the insulating layer over the photosensitive regions; and

removing a third portion of the insulating layer over the second set of diffusion regions in the periphery, leaving a spacer on at least one side of at least one gate structure of the second set of gate structures in the periphery.

26. (Original) The method of claim 25, wherein the gate structure of each said first and second sets of gate structures comprises a gate oxide and a gate conductor.

27. (Original) The method of claim 26, wherein the gate conductor comprises at least one of a polysilicon, silicide, metal, or combination of a polysilicon, silicide, and metal.

28. (Original) The method of claim 26, wherein the gate structure comprises a second insulator over the gate conductor.

29. (Original) The method of claim 28, wherein the second insulator comprises at least one of an oxide, nitride, metal oxide, or combination of an oxide, nitride, and metal oxide.

30. (Original) The method of claim 25, wherein each spacer is formed by a masked spacer etch.

31. (Currently amended) The method of claim 25, further comprising implanting dopant with each spacer used as a mask.

32. (Original) The method of claim 31, wherein the mask used to define the masked spacer etch remains during the dopant implantation.

33. (Original) The method of claim 25, wherein the insulating layer has a thickness within the range of about 100 to about 1500 Angstroms.

34. (Original) The method of claim 33, wherein the insulating layer has a thickness within the range of about 200 to about 1000 Angstroms.

35. (Original) The method of claim 31, wherein the dopant is an n-type dopant.

36. (Original) The method of claim 25, wherein the gate structures are comprised of at least one of an n-channel gate and a p-channel gate.

37. (Original) The method of claim 25, wherein the imaging device is a CMOS imager.

38. (Original) The method of claim 37, wherein the CMOS imager comprises a three-transistor, four-transistor, five-transistor, six-transistor, or seven-transistor architecture.

39. (Original) The method of claim 37, wherein the CMOS imager comprises at least one of a transfer gate, reset gate, row select gate, storage gate, dual conversion gate, and high dynamic range gate.

40. (Original) The method of claim 25, wherein the imaging device is a CCD imager.

41. (Original) The method of claim 25, wherein the insulating layer is selected from the group consisting of an oxide, nitride, oxide/nitride, and metal oxide.

42. (Original) The method of claim 25, wherein each of the first and second sets of diffusion regions is selected from the group consisting of a floating diffusion, N<sup>+</sup> active area, P<sup>+</sup> active area, N<sup>-</sup> active area, P<sup>-</sup> active area, and storage node diffusion.

43. (Original) The method of claim 42, wherein the first portion of the insulating layer is removed from over at least one of the floating diffusion, N<sup>+</sup> active area, P<sup>+</sup> active area, N<sup>-</sup> active area, P<sup>-</sup> active area, and storage node diffusion.

44. (Original) The method of claim 25, wherein the first and third portions of the insulating layer are removed by spacer etching.

45. (Original) The method of claim 25, wherein the first and third portions of the insulating layer are removed by at least one of an anisotropic dry etch and an isotropic etch.

46. (Original) The method of claim 25, wherein the imaging device has periphery circuits.

47. (Currently amended) The method of claim 25, further comprising implanting dopant with each spacer used as a mask.

48. (Original) The method of claim 25, wherein each spacer is left on at least one side of at least one gate structure.

49. (Original) The method of claim 25, wherein each spacer is left on both sides of at least one gate structure.

50. (Original) The method of claim 25, wherein each of the photosensitive regions is selected from the group consisting of a photodiode, photogate, and photoconductor.

51. (Original) The method of claim 50, wherein the photodiode is a p-n-p photodiode.

52. (Currently amended) A method of producing an imaging device, comprising:

forming photosensors and gate structures for N-channel transistors within a pixel array, and forming gate structures for N-channel and P-channel transistors outside said pixel array;

forming a spacer material over said photosensors and gate structures;

forming a first mask layer that covers said photosensors and gate structures for P-channel transistors and does not cover at least one of said gate structures for N-channel transistors;

etching said spacer material to form at least one sidewall spacer on at least one ~~of said gate structure~~ structures for an N-channel transistor, wherein said photosensors remain covered with said spacer material and said first mask layer;

implanting dopant to form N type source/drain regions for at least one N-channel transistor;

forming a second mask layer that covers said photosensors and gate structures for N-channel transistors and does not cover at least one of said gate structures for P-channel transistors;

etching said spacer material to form at least one sidewall spacer on at least one gate structure for a P-channel transistor, wherein said photosensors remain covered with said spacer material; and

implanting dopant to form P type source/drain regions for at least one P-channel transistor.

53. (Original) The method of claim 52, wherein each of said gate structures comprises a gate oxide and a gate conductor.

54. (Original) The method of claim 53, wherein the gate conductor comprises at least one of a polysilicon, silicide, metal, or combination of a polysilicon, silicide, and metal.

55. (Original) The method of claim 53, wherein each of said gate structures comprises a second insulator over the gate conductor.

56. (Original) The method of claim 55, wherein the second insulator comprises at least one of an oxide, nitride, metal oxide, or combination of an oxide, nitride, and metal oxide.

57. (Original) The method of claim 52, wherein the spacer material has a thickness within the range of about 100 to about 1500 Angstroms.

58. (Original) The method of claim 57, wherein the spacer material has a thickness within the range of about 200 to about 1000 Angstroms.

59. (Original) The method of claim 52, wherein the imaging device is a CMOS imager.

60. (Original) The method of claim 59, wherein the CMOS imager comprises a three-transistor, four-transistor, five-transistor, six-transistor, or seven-transistor architecture.

61. (Original) The method of claim 52, wherein the spacer material is selected from the group consisting of an oxide, nitride, oxide/nitride, and metal oxide.

62. (Original) The method of claim 52, wherein each of the photosensors is selected from the group consisting of a photodiode, photogate, and photoconductor.

63. (Original) The method of claim 52, wherein implanting dopant to form N type source/drain regions comprises implanting with phosphorus, arsenic or antimony.

64. (Original) The method of claim 63, wherein said dopant is implanted at a dose of about  $5 \times 10^{14}$  atoms/cm<sup>2</sup> to about  $5 \times 10^{16}$  atoms/cm<sup>2</sup>.

65. (Original) The method of claim 52, wherein implanting dopant to form P type source/drain regions comprises implanting with boron, boron-difluoride or indium.

66. (Original) The method of claim 65, wherein said dopant is implanted at a dose of about  $5 \times 10^{14}$  atoms/cm<sup>2</sup> to about  $5 \times 10^{16}$  atoms/cm<sup>2</sup>.

Claims 67-83 (Canceled).

84. (New) A method of producing an imaging device, comprising:

forming a photosensitive region;

forming a diffusion region;

forming a gate stack between said photosensitive region and said diffusion region;

forming an insulating layer over said photosensitive region, said gate structure and said diffusion region; and

forming at least one sidewall spacer on a first side of said gate stack by removing a first portion of said insulating layer, wherein a second portion of said insulating layer continuously covers said photosensitive region and a second side of said gate stack.

85. (New) A method of producing an imaging device, comprising:

forming a photosensitive region;

forming a gate structure adjacent to said photosensitive region;

forming an insulating layer over said photosensitive region and said gate structure;

removing a portion of the insulating layer over said gate structure, wherein said removed insulating layer portion exposes a first portion of a top surface of said gate structure, and wherein the remaining portion of said insulating layer covers a second portion of said top surface of said gate structure.